
PGP --> IDC REUSE MOVE SUMMARY SHEET FOR: 06004754 - 08/30/04 0019 Of 0034

Report Date/Time: 09/02/04 - 15:54

Created TEXTFILE: 60047545.001

Patent Contains Text Only.

VALID

Pat. No. 06004754 - 5
Issue Date: 08/30/04

Group ID: D
User ID: SXHolt
Page 1
KS: 12,523

Warning [Pages Of US References:]

page 7 has no references
page 8 has no references
page 9 has no references
page 10 has no references
page 11 has no references
page 12 has no references

Warning [Pages Of Foreign References:]

page 1 has no references
page 3 has no references
page 4 has no references
page 5 has no references
page 6 has no references
page 7 has no references
page 8 has no references
page 9 has no references
page 10 has no references
page 11 has no references
page 12 has no references

Warning [Pages Of Other References:]

position 1 on page 12 may be a duplicate because the first 75
characters are the same as position 2 on page 12

102

CHECK LIST

Rule 47 Continuing Data PCT Disclaimer

No ADS No Yes —

Microfiche Appendix CPA tag

No No —

Foreign Priority Claimed: No —

Acknowledged: No

Text Endorsement: 10086197.030102 —

=====

JACKET

<u>SERIAL NUMBER</u>	<u>FILING DATE</u>	<u>CLASS</u>	<u>SUBCLASS</u>	<u>GAU</u>
10/086,197	03/01/02	712	23	2154

FOREIGN PRIORITY
Country Document Number Date —

DISCLAIMER

/ /

TITLE

Superscalar RISC instruction scheduling —

MICROFICHE APPENDIX

ASSISTANT EXAMINER:

First: Middle: Last:

PRIMARY EXAMINER:

First: Middle: Last:

Larry D. Donaghue —

CLAIMS ALLOWED
Total Print

19 1

DRAWINGS

Sheets Figures Print

9 11 Y

=====

BLUE SLIP INFORMATION

<u>SERIAL NUMBER</u>	<u>CLASS</u>	<u>SUBCLASS</u>	<u>GAU</u>
10/086,197	712.	23	2154

<u>INDEP. CLAIMS</u>	<u>TOTAL CLAIMS</u>
1,13	19

=====

BLUE SLIP (Page 1)

INTERNATIONAL CLASSIFICATION

Class SubClass

G06F 9/38

CROSS-REFERENCES

Class SubClass

712 218;216

=====

TERM EXTENSION

0

FIELD OF SEARCH

Class SubClass

712 23;218;217;216

=====

OATH

INVENTOR NAME

First:

Middle:

Last:

Signed:

Sanjiv

Garg

Yes

City: Freemont

State: CA ZIP Code: Country: Foreign ZIP:

INVENTOR NAME

First: Middle: Last: Signed:

Kevin Ray Iadonato

Yes

City: San Jose

State: CA ZIP Code: Country: Foreign ZIP:

INVENTOR NAME

First: Middle: Last: Signed:

Le Trong Nguyen

Yes

City: Monte Sereno

State: CA ZIP Code: Country: Foreign ZIP:

INVENTOR NAME

First: Middle: Last: Signed:

Johannes Wang

Yes

City: Redwood City

State: CA ZIP Code: Country: Foreign ZIP:

=====
PCT INFO
=====

CONTINUING DATA (Page 1)

<u>LINE</u>	<u>CODE</u>	<u>SERIAL NUMBER</u>	<u>FILING DATE</u>	<u>STATUS</u>	<u>DOCUMENT NO.</u>	<u>ISSUE DATE</u>
104	71	09/906,099	07/17/2001	03		/ /
105	81	09/329,354	06/10/1999	01	6,289,433	/ /

106	81	08/990,414	12/15/1997	01	5,974,526	/	/
107	81	08/594,401	01/31/1996	01	5,737,624	/	/
108	81	08/219,425	03/29/1994	01	5,497,499	/	/
109	81	07/860,719	03/31/1992	03		/	/

=====

REFERENCES (Page 1) SERIAL NUMBER: 10/086,197
FORM 892

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
5,737,624	04/1998	Garg et al.	712	23
4,574,349	03/1986	Rechtschaffen	712	209
5,355,457	10/1994	Shebanow et al.	712	218
5,448,705	09/1995	Nguyen et al.	712	228
5,487,156	01/1996	Popescu et al.	712	217

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Popescu et al. The Metaflow Architecture pp. 10+13 B-638 IEEE Micro,
Jun. 1991.

=====

REFERENCES (Page 2) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
4,626,989	12/1986	Torii		
4,675,806	06/1987	Uchida		
4,722,049	01/1988	Lahti		
4,807,115	02/1989	Torng		

4,901,233 02/1990 Liptay —
4,903,196 02/1990 Pomerene et al. —
4,942,525 07/1990 Shintani et al. —
4,992,938 02/1991 Cocke et al. —
5,067,069 11/1991 Fite et al. —

FOREIGN REFERENCES

<u>Foreign</u>	<u>Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
0 515 166 A1		11/1992	EPX	—	
0 533 337 A1		03/1993	EPX	—	
WO 91/20031 A1		12/1991	WOX	—	

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Acosta, R. D. et al., +37 An Instruction Issuing Approach to Enhancing
Performance in Multiple Functional Unit Processors,+38 +0 +i IEEE
Transactions On Computers+1 , IEEE, vol. C-35, No. 9, Sep. 1986, pp.
815-828.

Agerwala, T. and Cocke, J., +i High Performance Reduced Instruction
Set Processors+1 , IBM Research Division, Mar. 31, 1987, pp. 1-61. —

Aiken, A. and Nicolau, A., +37 Perfect Pipelining: A New Loop
Parallelization Technique*,+38 +0 +i ESOP +3 88, 2nd European
Symposium on Programming+1 , Springer, ISBN 3-540-19027-9, 1988, pp.
221-235.

Butler, M. and Patt, Y., +37 An Improved Area-Efficient Register Alias
Table for Implementing HPS,+38 +0 University of Michigan, Ann Arbor,
Michigan, Jan. 23, 1990, 24 pages. —

Butler, M. et al., +37 Single Instruction Stream Parallelism Is
Greater Than Two, +38 +0 +i 18th Annual International Symposium on
Computer Architecture+1 , vol. 19, No. 3, ACM, May 1991, pp. 276-286.

=====

REFERENCES (Page 3) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
5,109,495	04/1992	Fite et al.		
5,142,633	08/1992	Murray et al.		
5,214,763	05/1993	Blaner et al.		
5,222,244	06/1993	Carbine et al.		
5,226,126	07/1993	McFarland et al.		
5,230,068	07/1993	Van Dyke et al.		
5,251,306	10/1993	Tran		
5,261,071	11/1993	Lyon		
5,345,569	09/1994	Tran		

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Charlesworth, A.E., +37 An Approach to Scientific Array Processing:
The Architectural Design of the AP-120B/FPS-164 Family,+38 +0 +i
Computer+1 , IEEE, vol. 14, Sep. 1981, pp. 18-27.

Colwell, R.P. et al., +37 A VLIW Architecture for a Trace Scheduling
Compiler,+38 +0 +i Proceedings of the 2nd International Conference on
Architectural Support for Programming Languages and Operating

Systems+1 , IEEE Computer Society, Oct. 1987, pp. 180-192. _____

Dwyer, H., III, Ph.D., +i A Multiple, Out-of-Order, Instruction
Issuing System For Superscalar Processors+1 , Dissertation for Cornell
University, UMI Dissertation Services, Aug. 1991, pp. iii-xvi and
1-249. _____

Foster, C.C. and Riseman, E.M., +37 Percolation of Code to Enhance
Parallel Dispatching and Execution,+38 +0 +i IEEE Transactions On
Computers+1 , IEEE, Dec. 1972, pp. 1411-1415. _____

Gee, J. et al., +37 The Implementation of Prolog via VAX 8600
Microcode,+38 +0 +i International Symposium on Microarchitecture:
Proceedings of the 19th Annual Workshop on Microprogramming+1 , ACM,
1986, pp. 68-74. _____

=====

REFERENCES (Page 4) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
<1,3>5,355,457	10/1994	Shebanow et al.		
5,398,330	03/1995	Johnson		
5,442,757	08/1995	McFarland et al.		
<1,4>5,448,705	09/1995	Nguyen et al.		
<1,5>5,487,156	01/1996	Popescu et al.		
5,497,499	03/1996	Garg et al.		
5,561,776	10/1996	Popescu et al.		
5,574,927	11/1996	Scantlin		

5,592,636

01/1997 Popescu et al.

FOREIGN REFERENCES

<u>Foreign</u>	<u>Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
----------------	----------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Goodman, J.R. and Hsu, W., +37 Code Scheduling and Register Allocation
in Large Basic Blocks, +38 +0 +i Proceedings of the 2nd International
Conference on Supercomputing+1 , ACM, 1988, pp. 442-452.

Gross, T.R. and Hennessy, J.L., +37 Optimizing Delayed Branches,+38 +0
+i Proceedings of the 5th Annual Workshop on Microprogramming+1 , IEEE
& ACM, Oct. 5-7, 1982, pp. 114-120.

Groves, R.D. and Oehler, R., +37 An IBM Second Generation RISC
Processor Architecture,+38 +0 +i Proceedings 1989 IEEE International
Conference on Computer Design: VLSI in Computers and Processors+1 ,
IEEE, Oct. 1989, pp. 134-137.

Horst, R.W. et al., +37 Multiple Instruction Issue in the NonStop
Cyclone Processor,+38 +0 +i Proceedings of the 17th Annual
International Symposium on Computer Architecture+1 , ACM, 1990, pp.
216-226.

Hwu, W. et al., +37 An HPS Implementation of VAX: Initial Design and
Analysis,+38 +0 +i Proceedings of the Nineteenth Annual Hawaii
International Conference on System Sciences+1 , 1986, pp. 282-291.

=====

REFERENCES (Page 5) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
5,625,837	04/1997	Popescu et al.		
5,627,983	05/1997	Popescu et al.		
5,708,841	01/1998	Popescu et al.		
<1,1>5,737,624	04/1998	Garg et al.		
5,768,575	06/1998	McFarland et al.		
5,778,210	07/1998	Henstrom et al.		
5,797,025	08/1998	Popescu et al.		
5,832,205	11/1998	Kelly et al.		
5,832,293	11/1998	Popescu et al.		

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Hwu, W. W. and Patt, Y.N., +37 Checkpoint Repair for High-Performance
Out-of-Order Execution Machines,+38 +0 +i IEEE Transactions On
Computers+1 , IEEE, vol. C-36, No. 12, Dec. 1987, pp. 1496-1514. _____

Hwu, W. and Patt, Y.N., +37 Design Choices for the HPSm Microprocessor
Chip,+38 +0 +i Proceedings of the Twentieth Annual Hawaii
International Conference on System Sciences+1 , 1987, pp. 330-336. _____

Hwu, W.W. and Chang, P.P., +37 Exploiting Parallel Microprocessor
Microarchitectures with a Compiler Code Generator,+38 +0 +i
Proceedings of the 15th Annual International Symposium on Computer
Architecture+1 , IEEE, Jun. 1988, pp. 45-53. _____

Hwu, W. and Patt, Y.N., +37 HPSm, a High Performance Restricted Data
Flow Architecture Having Minimal Functionality,+38 +0 +i Proceedings

of the 13th Annual Symposium on Computer Architecture+1 , IEEE, 1986,
pp. 297-306.

Hwu, W. and Patt, Y.N., +37 HPSm2: A Refined Single-chip
Microengine,+38 +0 Proceedings of +i HICSS-21-vol. I-Architecture+1 ,
1988, pp. 30-40.

=====

REFERENCES (Page 6) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
5,974,526	10/1999	Garg et al.		
*6,289,433	09/2001	Garg et al.		
No issue date available.				

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

+i IBM Journal of Research and Development+1 , IBM, vol. 34, No. 1,
Jan. 1990, pp. 1-70.

Johnson, W. M., +i Super-Scalar Processor Design+1 , Dissertation for
Stanford University, 1989, pp. ii-xiii and 1-134.

Jouppi, N.P. and Wall, D.W., +37 Available Instruction-Level
Parallelism for Superscalar and Superpipelined Machines,+38 +0 +i
Proceedings+13 3rd International Conference on Architectural Support
for Programming Languages and Operating Systems+1 , ACM, Apr. 1989,
pp. 272-282.

Jouppi, N.P., +37 The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance,+38 +0 +i IEEE Transactions on Computers+1 , IEEE, vol. 38, No. 12, Dec. 1989, pp. 1645-1658.

Melvin, S. and Patt, Y., +37 Exploiting Fine-Grained Parallelism
Through a Combination of Hardware and Software Techniques,+38 +0 +i

The 18th Annual International Symposium on Computer Architecture+1 ,
vol. 19, No. 3, ACM, May 1991, pp. 287-296.

Murakami, K. et al., +37 SIMP (Single Instruction stream/Multiple
instruction Pipelining): A Novel High-Speed Single-Processor
Architecture,+38 +0 +i Proceedings of the 16th Annual International
Symposium on Computer Architecture+1 , ACM, 1989, pp. 78-85.

=====

REFERENCES (Page 8) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
---------------------	-------------	-----------------	--------------	-----------------

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Peleg, A. and Weiser, U., +37 Future Trends in Microprocessors:
Out-of-Order Execution, Speculative Branching And Their CISC
Performance Potential+38 , IEEE, 1991, pp. 263-266.

Pleszkun, A.R. and Sohi, G.S., +37 The Performance Potential of
Multiple Functional Unit Processors*,+38 +0 +i Proceedings of the 15th
Annual International Symposium on Computer Architecture+1 , IEEE, Jun.
1988, pp. 37-44.

Pleszkun, A.R. et al., +37 WISQ: A Restartable Architecture Using
Queues,+38 +0 +i Proceedings of the 14th International Symposium on
Computer Architecture+1 , ACM, Jun. 1987, pp. 290-299.

Popescu, V. et al., +37 The Metaflow Architecture+38 , +i IEEE Micro+1

, IEEE, Jun. 1991, pp. 10-13 and 63-73.

Smith, M.D. et al., +37 Boosting Beyond Static Scheduling in a
Superscalar Processor,+38 +0 +i ACM SIGARCH Computer Architecture
News+1 , ACM, vol. 18, Issue 3, Jun. 1990, pp. 344-354. -----
=====

REFERENCES (Page 9) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
---------------------	-------------	-----------------	--------------	-----------------

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Patt, Y.N. et al., +37 Critical Issues Regarding HPS, A High
Performance Microarchitecture,+38 +0 +i Proceedings of the 18th Annual
Workshop on Microprogramming+1 , ACM, Dec. 3-6, 1985, pp. 109-116. -----

Patt, Y. et al., +37 Experiments with HPS, a Restricted-Data-Flow
Microarchitecture for High Performance Computers,+38 +0 +i COMPCON +3
86 digest of papers+1 , 1986, pp. 254-258. -----

Patt, Y.N. et al., +37 HPS, A New Microarchitecture: Rationale and
Introduction,+38 +0 +i Proceedings of the 18th Annual Workshop on
Microprogramming+1 , ACM, Dec. 1985, pp. 103-108. -----

Patt, Y.N. et al., +37 Run-Time Generation of HPS Microinstructions
From a VAX Instruction Stream,+38 +0 +i International Symposium on
Microarchitecture: Proceedings of the 19th Annual Workshop on
Microprogramming+1 , ACM, 1986, pp. 75-81. -----

Patterson, D.A. and Hennessy, J.L, +i Computer Architecture A
Quantitative Approach+1 , Morgan Kaufmann Publishers, Inc., 1990, pp.
xi-xv, 257-278, 290-314 and 449. ~~XXXXXXXXXX~~

=====

REFERENCES (Page 10) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
---------------------	-------------	-----------------	--------------	-----------------

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Smith, J.E. and Pleszkun, A.R., +37 Implementation of Precise
Interrupts in Pipelined Processors,+38 +0 +i Proceedings of the 12th
Annual International Symposium on Computer Architecture+1 , IEEE, Jun.
1985, pp. 36-44.

Smith, M.D. et al., +37 Limits on Multiple Instruction Issue,+38 +0 +i
Proceedings of the 3rd International Conference on Architectural
Support for Programming Languages and Operating Systems+1 , ACM, Apr..
1989, pp. 290-302.

Sohi, G. S. and Vajapeyam, S., +37 Instruction Issue Logic For
High-Performance, Interruptable Pipelined Processors,+38 +0 +i
Proceedings of the 14th Annual International Symposium on
Computer Architecture+1 , ACM, Jun. 2-5, 1987, pp. 27-34.

Swensen, J.A. and Patt, Y.N., +37 Hierarchical Registers for
Scientific Computers,+38 +0 +i Conference Proceedings: 1988

International Conference on Supercomputing+1 , ICS, Jul. 4-8, 1988,
pp. 346-353. ~~SE~~

Thornton, J.E., +i Design of a Computer: The Control Data 6600+1 ,
Control Data Corporation, 1970, pp. 58-140. ~~SE~~

=====

REFERENCES (Page 11) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
---------------------	-------------	-----------------	--------------	-----------------

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Tjaden, G.S. and Flynn, M.J., +37 Detection and Parallel Execution of
Independent Instructions,+38 +0 +i IEEE Transactions On Computers+1 ,
IEEE, vol. C-19, No. 10, Oct. 1970, pp. 889-895. ~~SE~~

Tjaden, G.S. and Flynn, M.J., +37 Representation of Concurrency with
Ordering Matrices,+38 +0 +i IEEE Transactions On Computers+1 , IEEE,
vol. C-22, No. 8, Aug. 1973, pp. 752-761. ~~SE~~

Tjaden, G.J., +i Representation and Detection of Concurrency Using
Ordering Matrices+1 , Dissertation for The Johns Hopkins University,
UMI Dissertation Services, 1972, pp. 1-199. ~~SE~~

Tomasulo, R.M., +37 An Efficient Algorithm for Exploiting Multiple
Arithmetic Units,+38 +0 +i IBM Journal of Research-and Development+1 ,
International Business Machines Corporation, vol. 11, No. 1, Jan.
1967, pp. 25-33. ~~SE~~

Uht, A.K., +37 An Efficient Hardware Algorithm to Extract Concurrency
From General-Purpose Code,+38 +0 +i Proceedings of the 19th Annual
Hawaii International Conference on System Sciences+1 , vol. I,
University of Hawaii, 1986, pp. 41-50.

=====

REFERENCES (Page 12) SERIAL NUMBER: 10/086,197
FORM 1449

U.S. REFERENCES

<u>U.S. Pat No.</u>	<u>Date</u>	<u>Patentee</u>	<u>Class</u>	<u>SubClass</u>
---------------------	-------------	-----------------	--------------	-----------------

FOREIGN REFERENCES

<u>Foreign Doc No.</u>	<u>Date</u>	<u>Country</u>	<u>Class</u>	<u>SubClass</u>
------------------------	-------------	----------------	--------------	-----------------

OTHER REFERENCE CITATIONS (incl. Author, Title, Date, Pertinent Pages, etc.)

Uvieghara, G.A. et al., +37 An Experimental Single-Chip Data Flow
CPU,+38 +0 +i IEEE Journal of Solid-State Circuits+1 , vol. 27, No. 1,
Jan. 1992, pp. 17-28.

Uvieghara, G.A. et al., +37 An Experimental Single-Chip Data Flow
CPU,+38 +0 +i Symposium on ULSI Circuits Design Digest of Technical
Papers+1 , May 1990, 2 pages.

Wedig, R.G., +i Detection of Concurrency In Directly Executed Language
Instruction Streams+1 , Dissertation for Stanford University, UMI
Dissertation Services, Jun. 1982, pp. ii, iii, v, vii-xv and 1-179.

Weiss, S. and Smith, J.E., +37 Instruction Issue Logic in Pipelined
Supercomputers,+38 +0 +i IEEE Transactions on Computers+1 , IEEE, vol.
C-33, No. 11, Nov. 1984, pp. 1013-1022 (77-86).

Wilson, J.E. et al., +37 On Tuning the Microarchitecture of an HPS

Implementation of the VAX,+38 +0 +i MICRO 20: Proceedings of the 20th
Annual Workshop on Microprogramming+1 , ACM SIGMICRO and IEEE CS
TC-MICRO, Dec. 1-4, 1987, pp. 162-167.

=====
